COLLEGE OF ENGINEERING
(AUTONOMOUS)

CMIS
BEYOND INNOVATION

VLSI SOCIETY OF INDIA

One Week Symposium on

Next-Gen VLSI Design for the Semiconductor Era:

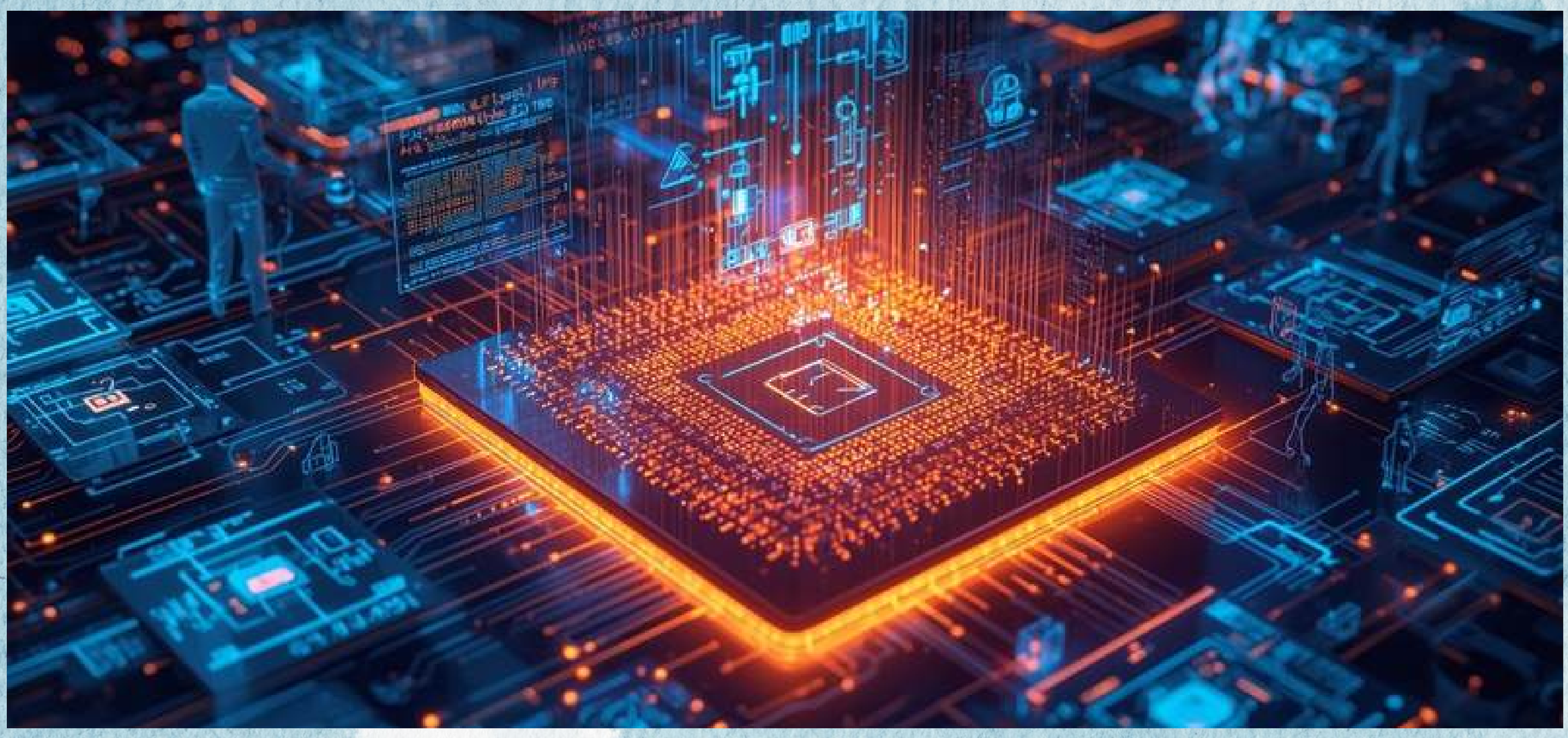
Current Trends, Challenges, and Hands-on Industry Training

9th to 13th March 2026

Jointly organized by

CENTRE FOR MEDICAL IMAGING STUDIES(CMIS),
DEPARTMENT OF ECE, GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING (A)
VISAKHAPATNAM, ANDHRA PRADESH

VLSI SOCIETY OF INDIA(VSI)
SEMICONDUCTOR MANUFACTURING
BANGALORE, KARNATAKA



Registration link: https://forms.gle/jDrZDL8tzNotqgkJ6

LAST DATE FOR REGISTRATION : 6TH MARCH 2026

GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING(A):-

Gayatri Vidya Parishad (GVP) has been established in the year 1988 as an educational trust by a group of eminent educationists, academicians & industrialists to empower the young generation through high quality technical education. The Engineering education by GVP society was first originated by establishing Gayatri Vidya Parishad College of Engineering (GVPCE) in the year 1996 with the divine blessings of Sadguru Sri.K. Sivananda Murthy Garu. The institute has flourished in various facets of Academics and Research by achieving the pinnacle of success. This institute is offering 11 B.Tech., 5 M.Tech., and one MCA programme under the affiliating university JNTUK, Kakinada. The college has brought in many initiatives for the benefit of students with autonomous status granted by UGC in 2009. The status of autonomy is further extended by UGC up to 2025. The institute has been reaccredited 3rd cycle by NAAC with A++ grade with CGPA of 3.52/4.0 for seven years. All the elgible B.Tech programs are accredited by NBA at least thrice.The institute received funds to the tune of Rs.5 Crores under Technical Education Quality Improvement Program (TEQIP), S.C-1.2. The college received Rs. 12 Crores from funding organizations AICTE/DST/NBHM/ARB etc. towards 45 R&D projects. The institute encourages collaborative learning between industry and academia as a means of reinforcing its curriculum with practical and real world experiences.

ABOUT SYMPOSIUM :-

This symposium aims to bridge the gap between academic learning and industry requirements in Next-Gen VLSI Design. With a focus on emerging trends, design challenges, and practical semiconductor applications, the program blends expert lectures with hands-on sessions using industry-standard EDA tools. Participants will gain cutting-edge insights and practical experience essential for research, teaching, and industry collaboration.

This symposium, conducted over five intensive days, will delve into the principles, practices, and emerging challenges of Next-Gen VLSI Design, with a strong emphasis on practical semiconductor industry applications. As the global semiconductor sector continues to expand at an unprecedented pace, the need for professionals with advanced VLSI design expertise has become critical.

Next-Gen VLSI circuits form the backbone of modern computing and electronics, enabling everything from consumer devices to high-performance processors and AI accelerators. Designing these circuits involves overcoming significant challenges such as power optimization, scalability, verification bottlenecks, and technology scaling. This symposium aims to provide a comprehensive platform for faculty, researchers, and industry professionals to explore theory, design methodologies, and hands-on training using industry-standard EDA tools, while academic knowledge provides the foundation, real-world VLSI design requires practical problem-solving skills to address issues such as power dissipation, timing closure, fabrication constraints, and design-for-testability (DFT). Through this program, participants will gain insights into current trends, research directions, and practical workflows that are directly relevant to the semiconductor industry.

Special focus will be given to ASIC and FPGA design flows, simulation, synthesis, and verification, along with exposure to low-power and high-performance design strategies. The Symposium also seeks to highlight the intersection of academia and industry, fostering research collaborations and enabling faculty to mentor students in industry-aligned projects.

This symposium aspires to establish itself as a premier academic–industry bridge program in the domain of Next-Gen VLSI design for the year 2026. By bringing together leading experts from industry and academia, the program will provide participants with the knowledge, skills, and resources to contribute meaningfully to the next wave of semiconductor innovation. Participants will engage in both theoretical sessions and hands-on practical training, gaining exposure to modern EDA tools and workflows widely adopted in semiconductor companies. The sessions will be led by distinguished resource persons, including VLSI researchers, semiconductor professionals, and tool experts, ensuring a rich blend of conceptual learning and industry-oriented application.

SESSION OBJECTIVES

- To introduce participants to the latest trends and innovations in Next-Gen VLSI design and semiconductor technologies.
- To provide an in-depth understanding of design methodologies, tools, and techniques used in practical VLSI design.
- To bridge the gap between academic concepts and industry practices in digital IC design.
- To develop hands-on skills in simulation, synthesis, verification, and implementation of VLSI circuits using industry-standard EDA tools.
- To highlight the challenges in low-power design, scaling, testing, and fabrication in modern semiconductor industries.
- To encourage research and project-oriented learning in advanced topics such as ASIC, FPGA, and SoC design.
- To build faculty competency for mentoring students in industry-relevant projects and research.

LEARNING OUTCOMES AT THE END OF THE SYMPOSIUM :

- Understand the current trends, challenges, and opportunities in Next-Gen VLSI design for semiconductor industries.
- Apply VLSI design methodologies in creating and testing digital circuits using simulation and synthesis tools.
- Demonstrate hands-on expertise in FPGA/ASIC design workflows using industry-standard EDA Tools.
- Analyze and solve design challenges related to low power, scalability, and performance optimization.
- Translate academic knowledge into practice by designing circuits aligned with real-world semiconductor applications.
- Guide students and researchers in carrying out innovative projects, research publications, and industry collaborations.
- Enhance career readiness by gaining skills aligned with the semiconductor and electronics industry demands.

VLSI SOCIETY OF INDIA (VSI):-

The VLSI Society of India was formed in 1989 with the noble goal of making India a strong force in VLSI. Activities in the VLSI area in India were limited at that time, and the number of professionals working in the VLSI area was also smaller. Now, over a hundred companies are working in India in the areas of chip design, embedded system design, electronic design automation, and design services.

A number of workshops, symposia, seminars, and conferences on VLSI-related topics are now being organized in India. The VLSI Design Conference, which has been sponsored by the VLSI Society of India, has grown significantly in the past 15 years, with the number of participants reaching 800. The VLSI Design and Test Workshops, another event sponsored by the VLSI Society of India, has also grown since its inception in 1998 and now attracts over 300 participants.

The purpose of the society is to contribute and promote the advancement of all aspects of VLSI technology, primarily in India, by all suitable means and in particular:

- To promote all areas relating to the VLSI field. This includes, but is not limited to, materials, technology, process, design, application, CAD/Design Automation, VLSI architectures, education, policies, etc.
- To bring a wide class of professionals from process technologies to specialists in VLSI architectures on one platform.
- To provide impetus to infrastructural growth for technology development.
- To provide impetus to human resources development.
- Conduct periodic seminars/conferences/workshops and such activities in this area.
- To bring out quality publications for effective dissemination of information.
- To continually formulate national goals for a sustained and vibrant VLSI industry.
- To evolve standards and frameworks for achieving effective synergy.
- To establish relations with other similar associations, national or international

ORGANIZING COMMITTEE

Chief Patron

Prof. Dr. Ing. P. S. Rao, President, GVP

Patrons

Sri D. Dakshina Murthy, Vice-President, GVP
Prof. K. P. R. Sastry, Vice-President, GVP
Prof. P. Somaraju, Secretary, GVP
Prof. Dr. A. B. Koteswara Rao, Principal, GVPCE

Chairman

Prof. Dr. Birendra Biswal, Dean (R&D), GVPCE

Convener

Dr. Leela Rani V, Associate Professor, GVPCE

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Dr. Bhaskararao J, Associate Professor, GVPCE

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Dr. D. B. V. Jagannadham, Professor, GVPCE
Dr. N. Deepika Rani, Professor & H.O.D, GVPCE

WHO CAN ATTEND :

- Students, Research Scholars, Faculty, Industry experts

PLATFORM: THE PROGRAM WILL BE CONDUCTED IN HYBRID MODE

OFFLINE VENUE: Gayatri Vidya Parishad College of Engineering(A), Kommadi, Visakhapatnam, 530048.

ONLINE PLATFORM: Google meet

The certificates will be jointly issued by both Gayatri Vidya Parishad College of Engineering, Visakhapatnam, Andhra Pradesh and VLSI Society of India (VSI) . The certificates will be sent to the registered mail ids to the delegates after successful participation in the workshop.

REGISTRATION FEE:

- Faculty/Industry Professionals: Rs.2500/-
- Research Scholars : Rs.1500/-
- Students: Rs.750/-

AGENDA

DAY-1 MONDAY, 9 MARCH 2026

10.30 AM to 12.00 PM

Er. DVR Murthy

Senior Vice President, MosChip

Topic: Possible Areas of Collaboration between Medical & Engineering Fields

1.00 PM to 4.00 PM

Er. Gyana Ranjan Khuntia

Associate Director, Siemens India Pvt. Ltd.

Topic: Fueling the Semiconductor Revolution: Convergence of HPC, 3DIC, and AI in Next-Gen VLSI Design

DAY-2 TUESDAY, 10 MARCH 2026

10.30 AM to 12.00 PM

Dr. Sounak Dey

Senior Scientist, TCS

Topic: Neuromorphic Computing: Applications, Hardware horizon and future directions

1.00 PM to 4.00 PM

Dr. Pradyut Biswal

Professor, IIIT Bhubhaneswar

Topic: Digital architecture for the implementation of Image processing algorithms in an FPGA

DAY-3 WEDNESDAY, 11 MARCH 2026

10.30 AM to 12.00 PM

Er. Sudheer Anumala

SoC Design Engineering Manager, Intel Corporation

Topic: Advanced DFT Methodologies: A Deep Dive into Scan, ATPG, and MBIST

1.00 PM to 4.00 PM

Er. Pooja Thotakura

Senior Silicon Design Engineer, AMD

Topic: Open-Source DFT Flow: A Hands-on Case Study from Simple RTL design to Patterns

DAY-4 THURSDAY, 12 MARCH 2026

10.30 AM to 12.00 PM

Dr. Kishor P. Sarawadekar

Associate Professor, IIT BHU

Topic: FPGA-based Accelerator Design for AI/ML Applications

1.00 PM to 4.00 PM

Dr. Ayaskanta Swain

Assistant Professor, NIT Rourkela

Topic: IoT on FPGA: A real time Embedded System Implementation

DAY-5 FRIDAY, 13 MARCH 2026

10.00 AM to 1.00 PM

Dr. Srinivas Boppu

Associate Professor, IIT Bhubhaneswar

Topic: Tsetlin Machine: Algorithm to Hardware

COORDINATORS:

1. **Dr. R. Surya Prakasa Rao**
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2. **Ms. Geetha Pavani. P**
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3. **Ms. Aswitha. R**
   Junior Research Fellow, GVPCE
4. **Mrs. K. Gayatri**
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